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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,652	05/27/2005	Swain Hong Alfred Yeo	1890-0250	7475

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MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
PATEL, REEMA	

ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,652	YEO ET AL.	
	Examiner	Art Unit	
	Reema Patel	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) was submitted on 9/26/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 11-12, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1).

5. Regarding claim 5, Lay et al. discloses the following claimed elements:

- A method of attaching a flip-chip to a substrate, the flip-chip including a first plurality of electrical contacts with lateral sides and the substrate including a second plurality of electrical contacts with lateral sides, the method comprising:
  - forming an insulating layer of an insulating material on the lateral sides of the first plurality of electrical contacts ([0023]);
  - joining the flip-chip to the substrate using a matrix of insulating material including conductive particles ([0023])

6. Yet, Lay et al. does not disclose forming an insulating layer or an insulating material on the lateral sides of the second plurality of electrical contacts ("bonding pads"). However, Wang et al. discloses forming an insulating layer ("solder mask") on the lateral sides of the bonding pads ([0033]). The purpose of such a step would be to prevent short-circuiting between bonding pads. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. with forming an insulating layer on the lateral sides of the bonding pads so as to prevent short circuiting between bonding pads.

7. Regarding claim 11, Lay et al. discloses joining the flip-chip to the substrate using a matrix of insulating material including conductive particles using an anisotropic conductive film ([0023]).

8. Regarding claim 12, Lay et al. discloses the following claimed elements:

- A flip-chip assembly comprising:
  - a flip chip having a first surface including a first plurality of electrical contacts, the first plurality of electrical contacts including lateral sides ([0023]);
  - a first electrically insulating film formed on the lateral sides of the first plurality of electrical contacts ([0023]);
  - a substrate having a second surface including a second plurality of electrical contacts, the second plurality of electrical contacts including lateral sides, and the second plurality of electrical contacts facing the first plurality of electrical contacts ([0023]);
  - a matrix of insulating material including electrically conductive particles between the flip chip and the substrate ([0023]).

9. Yet, Lay et al. does not disclose a second electrically insulating film formed on the lateral sides of the second plurality of electrical contacts. However, Wang et al. discloses forming an insulating layer ("solder mask") on the lateral sides of the bonding pads ([0033]). The purpose of such a step would be to prevent short-circuiting between bonding pads. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. with an insulating layer on the lateral sides of the bonding pads so as to prevent short circuiting between bonding pads.

10. Regarding claim 14, Lay et al. discloses that the matrix of insulating material including conductive particles is an anisotropic conductive film ([0023]).

11. Regarding claim 16, Lay et al. discloses that the first plurality of metal bumps comprise gold bumps ([0023], page 4 col 1 lines 1-2).

12. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1) as applied to claim 5 above, and further in view of Hendricks et al. (U.S. 6,153,525).

13. Regarding claim 6, Lay et al. discloses forming an insulating layer of silicon oxide ([0024]) on the lateral sides of the first plurality of electrical contacts. However, Hendricks et al. discloses that organic polymers have superior insulating characteristics as compared to those of silicon oxide. With using an insulative material comprising organic polymers, Hendricks et al. discloses a method of forming such a layer by coating a layer of the insulating material onto a surface, curing, and performing a polishing step (col 3, lines 15-24). The purpose of this method is to level the topography of the insulative layer and first plurality of electrical contacts. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. with using a polishing step, as taught by Hendricks et al. so as to level the topography of the insulative layer and first plurality of electrical contacts.

14. Regarding claim 7, Hendricks et al. discloses that the polishing is performed using CMP (col 3, lines 22-24) since such a process can rapidly remove elevated topographical features without significantly thinning flat areas (col 2, lines 10-15).

15. Regarding claim 8, Hendricks et al. discloses that the polishing is done using CMP and not by a backlapping tool. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a backlapping tool to polish the layer since the examiner takes Official Notice of the equivalence of backlapping and CMP for their use in the semiconductor art and the selection of any of these known equivalents to polish a film surface would be within the level of ordinary skill in the art.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1) as applied to claim 5 above, and further in view of Otsuki et al. (U.S. 5,846,853).

17. Regarding claim 9, Lay et al. in view of Wang et al. discloses forming an insulating layer on the lateral sides of a second plurality of electrical contacts but does not disclose the method of forming such a layer as recited in claim 9 of the instant application. However, Otsuki et al. discloses a patterning method in which a photosensitive layer of insulating material in coated onto a surface, exposed portions of the photosensitive layer are cured, and uncured portions of the photosensitive layer are removed (col 5, lines 23-31, 50-53). The purpose of such a method is to accurately deposit and selectively remove parts of a thin film. Therefore, it would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. in view of Wang et al. by using the patterning method as suggested by Otsuki so as to accurately form a patterned layer.

18. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1) as applied to claim 5 above, and further in view of Kitamura (U.S. 6,812,065 B1).

19. Regarding claim 10, Lay et al. discloses joining the flip-chip to the substrate using a matrix of insulating material including conductive particles using an anisotropic conductive film (ACF) but not an anisotropic conductive paste (ACP). However, Kitamura discloses that is preferable to use an ACP since it is less expensive than ACF due to less capital investment needed for and less waste generated during its production process (col 1, lines 22-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. in view of Wang et al. by using an ACP so as to reduce the expense related to the purchase of an anisotropic conductive material.

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1) as applied to claim 12 above, and further in view of Kitamura (U.S. 6,812,065 B1).

21. Regarding claim 13, Lay et al. discloses joining the flip-chip to the substrate using a matrix of insulating material including conductive particles using an anisotropic

conductive film (ACF) but not an anisotropic conductive paste (ACP). However, Kitamura discloses that is preferable to use an ACP since it is less expensive than ACF due to less capital investment needed for and less waste generated during its production process (col 1, lines 22-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. in view of Wang et al. by using an ACP so as to reduce the expense related to the purchase of an anisotropic conductive material.

22. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1) as applied to claim 12 above, and further in view of Vanfleteren (U.S. 6,555,414 B1).

23. Regarding claim 15, Lay et al. discloses that the substrate is a glass wafer ([0023]) and thus not a printed circuit board. However, Vanfleteren et al. discloses that the substrate used in a flip-chip assembly can be a printed circuit board so that the flip-chip assembly can be used in telecommunications applications (col 1, lines 20-21). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the substrate of the flip-chip assembly be a printed circuit board for use in telecommunications applications.

24. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1), Hendricks et al. (U.S. 6,153,525), and Otsuki et al. (U.S. 5,846,853).

25. Regarding claim 17, Lay et al. discloses the following claimed elements:

- A method of attaching a flip-chip to a substrate, the flip-chip including a first plurality of electrical contacts with lateral sides and the substrate including a second plurality of electrical contacts with lateral sides, the method comprising:
  - forming an insulating layer on the lateral sides of the first plurality of electrical contacts ([0023]);
  - joining the flip-chip to the substrate using a matrix of insulating material including conductive particles ([0023]).

26. Yet Lay et al. does not disclose the following:

a) forming the insulating layer on the lateral sides of the first plurality of electrical contacts by coating a layer of insulating material onto a surface of the flip-chip which includes the first plurality of electrical contacts, curing the layer of insulating material, and removing portions of the layer of insulating material overlying the first plurality of electrical contacts by chemical mechanical polishing;

b) forming an insulating layer of an insulating material on the lateral sides of the second plurality of electrical contacts

c) forming the insulating layer on the lateral sides of the second plurality of electrical contacts by coating a layer of photosensitive insulating material onto a surface of the substrate which includes the second plurality of electrical contacts, exposing portions of the layer of photosensitive insulating material which do not overlie the electrical contacts to

electromagnetic radiation in order to cure the portions of the layer of photosensitive insulating material which do not overlie the electrical contacts, and then removing uncured portions of the layer of photosensitive insulating material to expose the second plurality of electrical contacts;

27. Regarding (a), Lay et al. discloses forming an insulating layer of silicon oxide ([0024]) on the lateral sides of the first plurality of electrical contacts. However, Hendricks et al. discloses that organic polymers have superior insulating characteristics as compared to those of silicon oxide. With using an insulative material comprising organic polymers, Hendricks et al. discloses a method of forming such a layer by coating a layer of the insulating material onto a surface, curing, and performing a polishing step (col 3, lines 15-24). The purpose of this method is to level the topography of the insulative layer and first plurality of electrical contacts. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. with using a polishing step, as taught by Hendricks et al. so as to level the topography of the insulative layer and first plurality of electrical contacts.

28. Regarding (b), Lay et al. does not disclose forming an insulating layer or an insulating material on the lateral sides of the second plurality of electrical contacts ("bonding pads"). However, Wang et al. discloses forming an insulating layer ("solder mask") on the lateral sides of the bonding pads ([0033]). The purpose of such a step would be to prevent short-circuiting between bonding pads. Therefore, it would have

been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. with forming an insulating layer on the lateral sides of the bonding pads so as to prevent short circuiting between bonding pads.

29. Regarding (c), Lay et al. in view of Wang et al. discloses forming an insulating layer on the lateral sides of a second plurality of electrical contacts but does not disclose the method of forming such a layer. However, Otsuki et al. discloses a patterning method in which a photosensitive layer of insulating material in coated onto a surface, exposed portions of the photosensitive layer are cured, and uncured portions of the photosensitive layer are removed (col 5, lines 23-31, 50-53). The purpose of such a method is to accurately deposit and selectively remove parts of a thin film. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the patterning method as suggested by Otsuki so as to accurately form a patterned layer.

30. Regarding claim 19, Lay et al. discloses joining the flip-chip to the substrate using a matrix of insulating material including conductive particles using an anisotropic conductive film ([0023]).

31. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lay et al. (2002/0048924 A1) in view of Wang et al. (2004/0087057 A1), Hendricks et al. (U.S. 6,153,525), and Otsuki et al. (U.S. 5,846,853) as applied to claim 17 above, and further in view of Kitamura (U.S. 6,812,065 B1).

32. Regarding claim 18, Lay et al. discloses joining the flip-chip to the substrate using a matrix of insulating material including conductive particles using an anisotropic conductive film (ACF) but not an anisotropic conductive paste (ACP). However, Kitamura discloses that is preferable to use an ACP since it is less expensive than ACF due to less capital investment needed for and less waste generated during its production process (col 1, lines 22-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lay et al. in view of Wang et al. by using an ACP so as to reduce the expense related to the purchase of an anisotropic conductive material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SCOTT B. GEYER
PRIMARY EXAMINER

RSP
4/23/07

4/25/07